ABSTRACT

A method is provided for forming NMOS and PMOS transistors with ultra shallow source/drain regions having high dopant concentrations. First sidewall spacers and nitride spacers are sequentially formed on the sides of a gate electrode followed by forming a self-aligned oxide etch stop layer. The nitride spacer is removed and an amorphous silicon layer is deposited. The etch stop layer enables a controlled etch of the amorphous silicon layer to form silicon sidewalls on the first sidewall spacers. Implant steps are followed by an RTA to activate shallow and deep S/D regions. The etch stop layer maintains a high dopant concentration in deep S/D regions. After the etch stop is removed and a titanium layer is deposited on the substrate, an RTA forms a titanium silicide layer on the gate electrode and an extended silicide layer over the silicon sidewalls and substrate which results in a low resistivity.